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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,558	06/24/2003	Yasuhiro Shimada	60188-617	7768
7590	12/10/2004		EXAMINER	
Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street,, N. W. Washington, DC 20005-3096				LE, THAO X
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,558	SHIMADA ET AL.	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 November 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,3-8 and 10-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,3-8 and 10-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 2 and 9 are cancelled

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
4. Claims 1, 3-8, and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6727536 to Hasegawa et al in view of US 6491889 to Lee et al.

Regarding claims 1, Hasegawa discloses a memory device in fig. 2 comprising: a memory cell A100 with a capacitor 100 including a first electrode 12, column 7 line 25, a

Art Unit: 2814

ferroelectric film 14, column 7 line 21, and a second electrode 16, column 7 line 26, over the substrate 110.

But, Hasegawa does not disclose the memory wherein the ferroelectric film is made of a single crystal or a single domain.

However, Lee reference discloses the ferroelectric single crystal, column 3 line 4. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ferroelectric single crystal teaching of Lee to replace the ferroelectric material 14 of Hasegawa, because it would have created a memory cell having a high dielectric constant as taught by Lee, see column 3 line 4-6.

The process limitations " which are formed in this order, wherein the ferroelectric film is selectively grown ' of claim 1 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 3-4, the process limitation ' wherein the ferroelectric film is grown to be self-organized by physical or chemical interaction' of claim 3 and ' wherein the ferroelectric film is grown in a vapor phase or in a liquid phase' do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 5-7, Hasegawa discloses a memory device wherein the capacitor is connected to a selective switching device 112, wherein the selective switching device 112 is formed on the substrate or between the substrate and the first electrode, fig. 2, wherein the selective switching device is a transistor, column 8 line 24.

Regarding claim 8, Hasegawa discloses a memory device in fig. 30 comprising: a first capacitor array layer 100a including a plurality of capacitors each including a first electrode 12, a

Art Unit: 2814

first ferroelectric film 14 and a second electrode 16 which are formed over a substrate 110, and a second capacitor array 100b layer including a plurality of capacitors each including a third electrode 12, a second ferroelectric film 14 and a fourth electrode 16, over the substrate 110, the second capacitor array 100b layer being formed over the first capacitor array layer 100a with an insulating film 36, column 21 line 10, interposed between the first and second capacitor array layers.

The process limitations "which are formed in this order, wherein the ferroelectric film is selectively grown on the first electrode do not carry weight in a claim drawn to structure, wherein the second ferroelectric film is selectively grown on the third electrode' of claim 1 do not carry weight in the claim draw to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 10-11, the process limitations 'wherein the first ferroelectric film is grown to be self-organized by physical or chemical interaction and the second ferroelectric film is grown to be self-organized by physical or chemical interaction' and 'wherein each of the first and second ferroelectric films is grown in a vapor phase or in a liquid phase' do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 12-14, Hasegawa discloses a memory device wherein the capacitors constituting the first and second capacitor array layers are respectively connected to selective switching devices, 112, thereby forming respective memory cells, fig. 30, wherein each of the selective switching devices is formed on the substrate or between the substrate and the third electrode, fig. 30, wherein the selective switching devices are transistors, column 8 line 24.

Regarding claim 15, Hasegawa discloses a memory device wherein the selective switching device respectively connected to the capacitors constituting the second capacitor array layer are formed in the second capacitor array layer, fig. 30.

Regarding claim 16, Hasegawa does not disclose the switching device is a thin film transistor. However, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Hasegawa to connect to different devices for intended use, MPEP 2144.07.

Regarding claims 17-18, Hasegawa discloses the memory device, wherein means for electrically connecting the memory cells included in the second capacitor array layer to one another is provided between the first and second capacitor array layers or on the second capacitor array layer, wherein means for electrically connecting the memory cells included in the first capacitor array layer to the memory cells included in the second capacitor array layer is provided between the first and second capacitor array layers, fig. 30 and 32.

5. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6727536 to Hasegawa and US 6491889 to Lee et al as applied in the above claims 1 and 8 and further in view of US 6151240 to Suzuki.

Regarding claim 19-20, Hasegawa does not disclose the memory device wherein a lattice constant of crystals of the first electrode is substantially the same as that of the ferroelectric film, and, wherein a lattice constant of crystals of the first electrode is substantially the same as that of the first ferroelectric film and a lattice constant of crystals of the third electrode is substantially the same as that of the second ferroelectric film.

However, Suzuki discloses the memory structure in fig 1, wherein a lattice constant of crystals of the first electrode 3 is substantially the same as that of the single crystal ferroelectric film 4, column 16 lines 2 18-20. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the lattice matching of electrode and single crystal ferroelectric material teaching of Suzuki with Hasegawa's device, because it would have prevented the peel-off problem, improved fatigue property and reduced current leakage as taught by Suzuki, column 16 lines 24-31.

Response to Arguments

6. In response to applicant's argument that Lee is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Lee's reference is in the field of applicant's endeavor, i.e. a semiconductor device. It is evident that Lee discloses the ferroelectric single crystal having high dielectric constant, column 1 line 7, that can be used in the semiconductor devices such as actuator, ultrasonicator, optical modulators, and optical switches, column 1 lines 15-18. Although, Lee does not list capacitor device, but the application of ferroelectric material having high dielectric constant is not limited to the devices listed by Lee, but it is also can be used in other devices including the capacitor, which is well documented in the art, see Satoh (5576564), column 1 lines 15-27, Miyasaka (5053917), column 1 lines 25-40,

Art Unit: 2814

Kijima (5821005), column 1 lines 15-33. The Examiner submits that Lee's reference is an analogous art; thus the combination of Lee and Hasegawa is proper.

7. The 'wafer' is a generic term to indicate a thin disk or ring resembling a wafer or a thin slice of semiconductor substrate normally comprising silicon used as a base for an electronic device fabrication.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

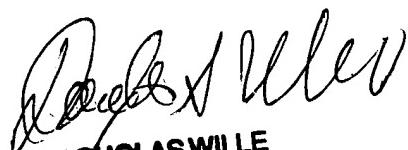
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
26 Nov. 2004



DOUGLAS WILLE
PRIMARY EXAMINER